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CS33

Third Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. With suitable example explain: i) Boolean function ii) Maximum canonical formula iii) Incomplete Boolean function. **(06 Marks)**

b. Show the realization of the following:
i) NOR using NAND gates ii) X-NOR using NAND gates. **(10 Marks)**

c. Draw the logic diagram using basic gates of the following Boolean function:
$f(A,B,C,D) = \overline{A(B(CD+\overline{E})+\overline{CE})} + \overline{A}\,\overline{B}$ assuming input variables are available in uncomplemented and complemented form. **(04 Marks)**

2 a. Differentiate between positive, negative and mixed logic. Give example for each case. **(06 Marks)**

b. Prove that: i) $x + \overline{x}y = x + y$ ii) $ab + \overline{ac} + a\overline{b}c(ab+c) = 1$. **(08 Marks)**

c. Simplify using Karnaugh map method and realize the simplified function using NAND gates.
$f(x,y,z) = \sum m(0,1,4) + \sum dc(3,7)$. **(06 Marks)**

3 a. Design a minimal two level gate combinational network that detects the presence of six illegal code group in a 4-bit that represent 8421 BCD code, by providing logic 1 output. **(10 Marks)**

b. Simplify the following switching function using Quine-Mccluskey method:
$f(A,B,C,D) = \sum m(1,3,13,15) + \sum dc(8,9,10,11)$. **(10 Marks)**

4 a. Define: i) Propagation delay ii) Power-delay product iii) Fan-out iv) Noise margin. **(04 Marks)**

b. Write the circuit diagram of a TTL NAND gate and draw and explain the transfer characteristic. **(07 Marks)**

c. Explain with respect to TTL the following output stages:
i) Totem pole ii) Open collector iii) Tri-state output. **(09 Marks)**

5 a. Draw the circuit of a JK-flipflop using NAND gates building blocks. Verify that JK-flipflop satisfy the difference equation: $Q_{n+1} = J_n\overline{Q}_n + \overline{K}_nQ_n$. **(10 Marks)**

b. Show how JK-flipflop can be connected as i) D-flipflop ii) T-flipflop. **(06 Marks)**

c. Describe a C-MOS inverter with relevant circuit diagram. **(04 Marks)**

6 a. Differentiate between ripple and synchronous counter. **(04 Marks)**

b. Design a synchronous module-S counter and sketch the output waveform. **(08 Marks)**

c. With a block diagram describe a 3-bit Johnson twisted ring counter. Draw the sequence diagram and indicate the valid and invalid states. **(08 Marks)**

7 a. Discuss what is race – around in JK-flipflop and describe: i) Master – slave JK-flipflop ii) Edge triggered flipflop. **(12 Marks)**

b. Design suitable circuit for the output of truth table shown in the table below using i) 8:1 Multiplexer ii) 4:1 Multiplexer. **(08 Marks)**

Inputs			Outputs
A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

8 Write short notes on any three of the following:
a) Priority encoder b) CMOS in comparison with TTL family c) Magnitude comparator
d) Programmable array logic. **(20 Marks)**